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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,425	06/26/2003	H. Bernhard Pogge	FIS920000134US3	6336

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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,425	POGGE ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Tokuda et al. (US Pat. 5870289) in view of Ahn et al. (US Pat. 6586835).

Regarding claims 17, 19 and 20, Tokuda et al. disclose a semiconductor device/stacked module (Fig. 6) including a plurality of chips (see 411-1, 411-2, etc. in Fig. 6) including active devices and having front/bottom and back/top surfaces, the device comprising:

- a plate/support (510 in Fig. 6) being positioned/attached to the chips on/over the back surfaces thereof
- the chips being arranged on/over the support in a planar horizontal structure with adhesive material/filling (see 461-1, 461-2, etc. in Fig. 6) between the chips
- a first layer/adhesive layer (421-1 in Fig. 6) having first/bottom and second/top surfaces being disposed on the front surfaces of the chips and having a plurality of filled vias/through-holes (see 441-1 in Fig. 6) having respective electrically conductive material/studs therein

- conducting pads (not numerically referenced in Fig. 6- see 11/21 in Fig. 1) in registration with the respective filled vias/studs
- a second layer/chip carrier/wiring substrate (451-1 in Fig. 6) attached to the first layer on the second surface of the first layer, the second layer being formed of a solid dielectric/printed wiring board substrate (see 20 in Fig. 1; Col. 13, line 45; Col. 14, line 63) and having conductive pads and wiring/traces (not numerically referenced in Fig. 6- see 21/40 within layer 20 in Fig. 1) in registration with respective vias/studs, the wiring/traces on/within the second layer (see the wiring including vias/pads/traces within and on 451-1 in Fig. 6) further electrically interconnecting the pads of the plurality of chips with each other (Fig. 6; Col. 20, lines 1-15) and with the plurality of chip carriers/wiring substrates through through-holes (see 470 in Fig. 6) in the stacked module

(Fig. 6; Fig 1-6; Col. 19, line 45- Col. 21, line 35; Col. 11-21).

Tokuda et al. fail to teach the chips including a chip without active devices.

Ahn et al. teach an integrated circuit (IC) device package including a plurality of chips (see 125A, 125AA, 125B, etc. in Fig. 1A) having a variety of types and sizes (DRAM, logic, passive, etc.), the chips including active devices and that without active devices comprising passive devices/components and being positioned/coupled according to the desired order/pattern with respect to each other (see Col. 4, line 60- Col. 5, line 33).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the chips including a chip without active devices and that having a size according to a placement pattern of the chips with active devices as taught by Ahn et al. so that the system integration and electrical performance can be improved in Tokuda et al's device.

Regarding claim 18, Tokuda et al. and Ahn et al. teach substantially the entire claimed structure as applied to claim 17 above, wherein Tokuda et al. further teach an attachment layer/laminated substrate (see 430/420/460 in Fig. 6) between the support and the chips, the attachment layer having a plurality of support connection via/pads and studs (see 440 in Fig. 6; also see 40/21 in Fig. 1) formed in registration therewith having respective interconnections (Col. 20).

Response to Arguments

3. Applicant's arguments with respect to claims 17-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

06-07-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800